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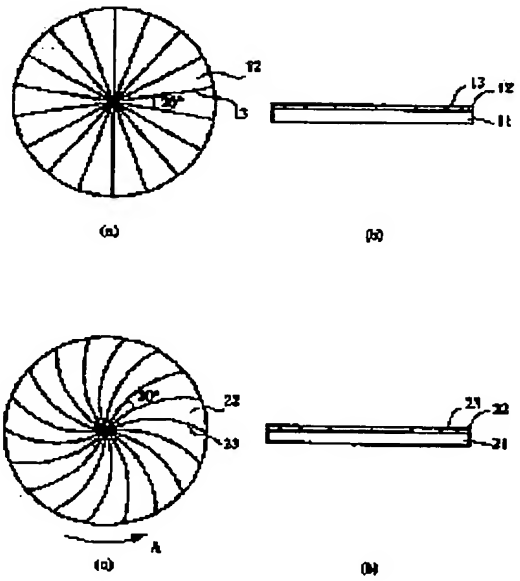
(54) MANUFACTURE OF SEMICONDUCTOR DEVICE AND ABRASIVE DEVICE

(57)Abstract:

PURPOSE: To lessen a difference between the abrasive wears of the peripheral part and the central part of a wafer to conduct a flattening of the peripheral part and the central part and to prevent the generation of a short-circuit between wirings by a method wherein grooves are provided in an abrasive cloth adhered on the platen of an abrasive device in a radial form from the center of the cloth for improving the drainage of an abrasive liquid.

CONSTITUTION: The structure of an abrasive cloth is constituted of a several mm-thick polyurethane 11 and about 1mm-thick abrasive pads 12 adhered oh the surface of the polyurethane 11. The fan-shaped abrasive pads 12 are adhered on the surface of the polyurethane 11. Intervals of 2mm or thereabouts are respectively provided between the pads 12 so that an abrasive liquid flows well, whereby grooves 13 are provided in the abrasive cloth in a radial form from the center of the abrasive cloth. Thereby, the abrasive liquid flows from the central part of a platen to the outer periphery of the platen via the grooves provided in the abrasive cloth by a centrifugal force which is generated by the rotation of the platen.



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* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] The manufacture approach of the semiconductor device characterized by providing the process which prepares for a front face the semi-conductor substrate which has a level difference, the process which forms an insulating layer on said level difference front face, and the process which grinds said insulator layer with the abrasive cloth which has a slot in a radial.
[Claim 2] The manufacture approach of the semiconductor device characterized by providing the process which forms the conductive layer connected with the predetermined conductivity-type field in a semi-conductor substrate, the process which forms the insulating layer which covers said conductive layer, the process which covers said wiring layer and forms an insulating layer on said semi-conductor substrate, and the process which grinds said insulator layer with the abrasive cloth which has a slot in a radial.
[Claim 3] The manufacture approach of the semiconductor device characterized by providing the process which prepares the semi-conductor substrate of a predetermined conductivity type, the process which forms a slot in the predetermined field of said semi-conductor substrate, the process which forms an insulator layer on said semi-conductor substrate front face including the interior of said slot, and the process which grinds said insulator layer with the abrasive cloth which has a slot in a radial.
[Claim 4] In the manufacture approach of a semiconductor device claims 1 or 2 or given in three The slot of the radial of said abrasive cloth is the manufacture approach of the semiconductor device characterized by curving to the opposite direction to the hand of cut of said abrasive cloth.
[Claim 5] In the manufacture approach of a semiconductor device claims 1 or 2 or given in three The process which grinds said insulator layer is the manufacture approach of the semiconductor device characterized by being carried out by the chemical polish with polish liquid, and the mechanical polish by polish liquid and abrasive cloth.
[Claim 6] It is polish equipment characterized by said abrasive cloth having the slot on the radial in the polish equipment which has the rolling mechanism which carries out rotation sliding of the substrate supporter which supports the substrate which has the insulating layer which covers a conductive layer and said conductive layer, the abrasive cloth which grinds said substrate front face, the surface plate which fixed said abrasive cloth removable, and said substrate and said abrasive cloth relatively.
[Claim 7] It is polish equipment characterized by the slot of the radial of said abrasive cloth curving to the opposite direction to the hand of cut of said platen in polish equipment according to claim 6.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the manufacture approach of the manufacture approach of a semiconductor device, polish equipment, especially the semiconductor device that requires a flattening technique, and polish equipment.
[0002]
[Description of the Prior Art] Multilayering of wiring formed in detailed-izing and the component of a semiconductor device is progressing in recent years. Therefore, flattening of the semi-conductor substrate (wafer is called hereafter.) front face is carried out, and in order to promote detailed-izing and multilayering of wiring, improvement in a flattening technique is demanded. While being this flattening technique, let the CMP (Chemical and Mechanical Polishing) method be an effective technique in respect of that effectiveness and cost. The CMP method is the approach of grinding abrasives-ed mechanically by the particle contained in polish liquid at the same time it grinds by giving the capacity which etches abrasives-ed into polish liquid chemically.
[0003] Then, the structure of the polish equipment used for the CMP method is explained with reference to drawing 4 . Polish equipment has the wafer attaching part which fixes a polish base and a wafer, and the part which supplies polish liquid, and the polish base has the abrasive cloth 102 stuck on a platen 101 (surface plate) and its front face. Moreover, a wafer attaching part fixes a wafer by attracting a wafer 104 from the vacuum hole 103. The part which supplies polish liquid has the nozzle 105 for slurries, and the pure-water nozzle 106.
[0004] An above-mentioned wafer attaching part and an above-mentioned platen rotate, and a wafer attaching part descends and it is carried [in / both / the flattening process of a wafer] out by contacting the front face of a wafer to the abrasive cloth on a platen, and pressurizing it. In this process, it is important to optimize the amount of etching of chemical polish and the balance of the pressurization of mechanical polish in consideration of the surface state of a wafer. The amount of polishes of chemical polish is determined by conditions, such as a class of polish liquid, pH, and a presentation. Moreover, the amount of polishes of mechanical polish is determined by the conditions of the class of particle contained in polish liquid, concentration, abrasive cloth, a pressure, rotational speed, a hand of cut, etc.
[0005] however, the thing for which the above-mentioned conditions are controlled -- not easy -- between wafers -- or dispersion arises in the amount of polishes in the same wafer. It is because a wafer center section will be especially ground quickly since it says that the amount of polishes of dispersion in the amount of polishes in the same wafer increases in the center section of a wafer, the center section of a wafer tends to be covered with polish liquid as this cause and the amount of polishes increases in the center section of a wafer for this reason. The effective cure for preventing this is difficult for the control few. Therefore, a trouble as shown below arises in the production process of a semiconductor device.
[0006] In the production process of a semiconductor device, the case where the CMP method is applied in the flattening process of an interlayer film is first explained with reference to drawing 5 as the first example. As first shown in drawing 5 (a), in order to form the first interlayer film 152 and to form the first wiring layer 153 on wafer 151 front face, 6000A aluminum film is formed and patterning of this is carried out.
[0007] Then, as shown in drawing 5 (b), silicon oxide of 10000A of thickness is formed as the second interlayer film 154 on aluminum film 153 front face and the first exposed interlayer film 152 front face. Then, flattening of the second interlayer film is performed using the CMP method.
[0008] In the center section of the wafer which the flattening process ended, since polish liquid collects mostly and the amount of polishes increases, as shown in drawing 5 (c), the second interlayer film 153 on

the first wiring layer 153 is ground too much, and the front face of the first wiring layer 153 may become unreserved.

[0009] If aluminum film is formed as the second wiring layer 155 on a front face in this condition, as shown in drawing 5 (d), in the center section of a wafer, the first wiring layer 153 and second wiring layer 155 will contact, and the problem that the first wiring layer and second wiring layer short-circuit will arise.

[0010] Even if the front face of the first wiring layer 153 does not become unreserved in the center section of a metaphor wafer, in the center section and periphery of a wafer, the amounts of polishes of the second interlayer film 154 will differ, and a difference will arise in the thickness of the interlayer films 152 and 154 from a wafer 151. When it is going to form contact to a wafer 151 in this condition, if control of etching by the RIE method in the center section and periphery of a wafer 151 is difficult and etches according to a periphery with the thick thickness of interlayer films 152 and 154, in the center section where the thickness of interlayer films 152 and 154 is thin, even a wafer 151 will reach and etching will give a damage to a wafer. On the contrary, if the thickness of interlayer films 152 and 154 etches according to a thin center section, in a periphery with the thick thickness of interlayer films 152 and 154, ** which forms contact of sufficient depth for interlayer films 152 and 154 will become difficult.

[0011] Moreover, in the flattening process of the embedding component detached core in the production process of a semiconductor device, the case where the CMP method is applied is explained with reference to drawing 6 as the second example. it is first shown in drawing 6 (a) -- as -- a wafer 161 front-face top -- the oxide film 162 of 500A of thickness -- minding -- as the stopper film -- the polycrystal silicone film 163 of 2000A of thickness -- forming membranes -- the polycrystal silicone film 163 on the formation schedule field of a component detached core, an oxide film 162, and a wafer 161 -- RIE (Reactive Ion Ecthing) -- it etches by law and the trench 164 with a depth of about 6000A is formed.

[0012] Then, as shown in drawing 6 (b), the oxide film 165 of 10000A of thickness is formed in a trench and on polycrystal silicone film 163 front face as embedding material. Then, flattening of an oxide film 165 is performed using the CMP method.

[0013] Although it leaves the polycrystal silicone film 163 which is stopper film and a flattening process is ended in the periphery of the wafer which the flattening process ended, since polish liquid collects mostly and the amount of polishes increases as the center section of a wafer is shown in drawing 6 (c), the polycrystal silicone film 163 may be ground completely and even a wafer 161 may be ground.

[0014] In etching which exfoliates the polycrystal silicone film 163 and an oxide film 162 and which is performed for accumulating, if manufacture of a semiconductor device is continued like usual in this condition, since the wafer front face is exposed, a wafer 161 will be etched and a damage will be received in the center section of a wafer. For this reason, as shown in drawing 6 (d), in the wafer of a wafer center section, especially the boundary section with a component detached core, a defect may arise and the rearrangement 167 may have arisen. When carrying out like ion grouting for forming an impurity range 166, the problem of generating junction leakage current produces this rearrangement 167.

[0015] Therefore, in order to protect, in consideration of dispersion in the amount of polishes in the center section and periphery of a wafer, it thickens thickness of the polycrystal silicone film 163 and is so thick that this dispersion is large, and it necessary to carry out that a wafer 161 is ground too much.

[0016] However, when the amounts of polishes of the polycrystal silicone film 163 or an oxide film 162 differ by the center section and periphery of a wafer 161, the level difference of height which is different by the center section and periphery of a wafer 161 around the oxide film 165 which will embed if these are removed, and is formed as a component layer arises. For example, when electric conduction film, such as WSi, is deposited on a wafer 161 and patterning of this is carried out, in the periphery of the wafer 161 with this high level difference, the problem of that the electric conduction film remains on the side attachment wall of a level difference, this electric conduction film that remained short-circuiting arises.

[0017] In the production process of the semiconductor device by the CMP method using conventional polish equipment, the polish liquid which grinds abrasives-ed remains in the center section of a wafer mostly as mentioned above, and the amounts of polishes differ in the periphery and center section of a wafer. for this reason -- for example, when contact of depth sufficient if the flattening process of an interlayer film is performed, when an interlayer film is ground too much in a wafer center section, and the short-circuit during wiring will arise or it will form contact cannot be formed, a wafer may be etched conversely

[0018] Moreover, when the junction leak which will consider the rearrangement in a wafer as a cause if a wafer will be ground in the center section of a wafer if flattening of an embedding component demarcation membrane is performed, a rearrangement arises and an impurity range is formed in a wafer by this occurs, or when carrying out patterning of the electric conduction film formed on the embedding component layer, this

electric conduction film may remain and short-circuit may arise.

[0019]

[Problem(s) to be Solved by the Invention] This invention aims at offering the manufacture approach of polish equipment which a difference does not produce in the amount of polishes in the periphery and center section of a wafer, and the semiconductor device which prevents the short-circuit during wiring, and generating of the junction leakage current by the rearrangement using the polish equipment in view of the above-mentioned trouble.

[0020]

[Means for Solving the Problem] In order to prevent polish liquid collecting mostly in the center section of a wafer in this invention in order to attain the above-mentioned purpose, the slot on the radial is established in the abrasive cloth stuck on the platen of polish equipment, the brush of polish liquid is raised, and it considers as the structure which the difference of the amount of polishes does not produce in the periphery and center section of a wafer. The flattening process of the interlayer film on a wafer and the flattening process of an embedding component demarcation membrane are collectively performed using this polish equipment.

[0021]

[Function] According to this invention, in the production process of a semiconductor device, when performing the flattening process of the interlayer film on a wafer, and the flattening process of an embedding component demarcation membrane using polish equipment, in order to raise the brush of polish liquid to the abrasive cloth stuck on the platen of polish equipment, the difference of the amount of polishes becomes possible [performing flattening few] in the periphery and center section of a wafer by preparing the slot on the radial. Therefore, in the flattening process of an interlayer film, an interlayer film is not ground too much and the short-circuit during wiring can be prevented. Moreover, in the flattening process of a component demarcation membrane, it becomes possible not to grind a wafer and to prevent generating of the junction leak by the rearrangement of a wafer. It becomes possible to suppress dispersion in processing produced at the process after being based furthermore on dispersion in the residual membrane after polish.

[0022]

[Example] The example of this invention is explained with reference to a drawing. The plan of the abrasive cloth in the first example of the polish equipment of this invention is first shown in drawing 1 (a), and a horizontal side Fig. is shown in drawing 1 (b). Moreover, about polish equipments other than abrasive cloth, it is the same as usual and an explanatory view is omitted. The material of abrasive cloth is the same as usual.

[0023] The structure of abrasive cloth consists of scouring pads 12 with a thickness of about 1mm stuck on polyurethane 11 with a thickness of several mm and its front face, and the scouring pad 12 of the sector of 16 sheets of 20 central angles is stuck on the front face of polyurethane 11. It has spacing of about 2mm between the scouring pads 12 of each sector, and, therefore, it has a total of 16 slots 13 in the radial from the core of abrasive cloth so that the brush of polish liquid may become good. Thereby, it is lost that the core of the wafer with which the flattening process is performed is mostly covered with polish liquid of polish liquid in order to flow from the core of a platen to a periphery via the slot between abrasive cloth according to the centrifugal force produced by rotation of a platen, and the trouble that the difference of the amount of polishes arises in the periphery and core of a wafer is solved.

[0024] Then, the plan of the abrasive cloth in the second example of this invention is shown in drawing 1 (c), and a horizontal side Fig. is shown in drawing 1 (d). The second example is based on the same material as the first example, and the configurations of the slot on the scouring pad differ. The scouring pad 22 on the polyurethane 21 front face in the second example has the slot 23 of the radial which curved in the fixed direction, it consists of scouring pads of 12 sheets of 20 central angles like the first example, has spacing of about 2mm between each scouring pad, and has a total of 16 slots in the radial which therefore curved from the core of abrasive cloth. Although the same effectiveness as the first example is acquired, the brush of polish liquid becomes good further by forming the slot which curved to the hand of cut and opposite direction of the platen shown by the arrow head A.

[0025] In the above-mentioned example, although abrasive cloth showed the example constituted by two-layer [of polyurethane and a scouring pad], it may constitute abrasive cloth from one layer of scouring pads. In this case, a slot with a depth of about 0.5-1mm is formed on a scouring pad with a thickness of about 1-2mm. Moreover, it is not limited to the number or include angle which were shown above, it deforms variously by the difference in a platen, the rotational speed of a wafer supporter, the condition of a polished surface-ed, the class of polish liquid, concentration, etc., and formation spacing of the number of a

slot or a slot formed with a scouring pad can be carried out.

[0026] Moreover, in the second example, although the example which gives and forms a curve in the slot formed with a scouring pad was shown, it is possible to deform variously by the difference between the rotational speed of a platen or a wafer supporter, the class of polish liquid, concentration, etc., and to carry out also with also whenever [curve].

[0027] Then, the example in the case of performing a flattening process in the production process of a semiconductor device is explained with reference to a drawing using the polish equipment shown above. As first shown in drawing 2 (a) as the first example of the manufacture approach, in order to form the first interlayer film 52 and to form the first wiring layer 53 on wafer 51 front face, 6000A aluminum film is formed, this is etched, and patterning is performed.

[0028] Then, as shown in drawing 2 (b), silicon oxide of 10000A of thickness is formed as the second interlayer film 54 on aluminum film 53 front face and the first exposed interlayer film 52 front face. Then, a wafer is set in the polish equipment by this invention, this is operated and flattening of the second interlayer film by the CMP method is performed.

[0029] In the core and periphery of the wafer which the flattening process ended, polish liquid cannot collect in the wafer center section mostly by work of the slot currently formed in the scouring pad, the difference of the amount of polishes can decrease by the center section and periphery of a substrate, and the structure where the second interlayer film 54 remains on the first wiring layer 53 front face by both the center sections and peripheries of a wafer as shown in drawing 2 (c) can be acquired.

[0030] Then, as shown in drawing 2 (d), it is formed when the second wiring layer 55 forms aluminum film. Since the interlayer film 54 is formed on the first wiring layer 53, pressure-proofing of the request during wiring is maintained.

[0031] Next, the case where the CMP method is applied in the flattening process of the embedding component detached core in the production process of a semiconductor device as the second example of the manufacture approach is explained with reference to drawing 3 .

[0032] As first shown in drawing 3 (a), on wafer 61 front face, through the oxide film 62 of 500A of thickness, the polycrystal silicone film 63 of 2000A of thickness is formed as stopper film of polishing, the polycrystal silicone film 63 on the formation schedule field of a component detached core, an oxide film 62, and a wafer 61 are etched, and the trench 64 with a depth of about 6000A is formed.

[0033] Then, as shown in drawing 3 (b), the oxide film 65 of 10000A of thickness is formed in a trench and on polycrystal silicone film 63 front face as embedding material. Then, a wafer 61 is set in the polish equipment by this invention, this is operated, and flattening of an oxide film 65 is performed.

[0034] In the core and periphery of the wafer which the flattening process ended, polish liquid cannot collect in the wafer center section mostly by work of the slot currently formed in the scouring pad, the difference of the amount of polishes in the center section and periphery of a wafer can decrease, and flattening can be mostly carried out to homogeneity. A wafer is not ground as both the center sections and peripheries of a wafer show to drawing 3 (c).

[0035] Then, as shown in drawing 3 (d), etching removes the polycrystal silicone film 63 and an oxide film 62, an impurity is poured into the predetermined field of a wafer 61, and an impurity range 66 is formed.

[0036] In the flattening process of these above-mentioned interlayer film, the difference of the amount of polishes can be decreased in the periphery and center section of a wafer by using the polish equipment by this invention. Therefore, flattening of a reliable wafer can be performed -- by etching used in order to remove a polycrystal silicone film and an oxide film, a wafer does not receive a damage, and even if a rearrangement does not arise but it forms an impurity range in a wafer, do not produce junction leak and the short-circuit between wiring layers does not arise further.

[0037]

[Effect of the Invention] The brush of polish liquid improves by establishing the slot on the radial in the **** abrasive cloth which is stuck on a platen according to this invention. Therefore, the difference of the amount of polishes becomes possible [performing flattening few] in the periphery and center section of a wafer. For example, in the flattening process of an interlayer film, while becoming possible not to grind an interlayer film too much, and not to grind a semi-conductor wafer in the flattening process of a component demarcation membrane, and to prevent the short-circuit during wiring, and generating of the junction leakage current by the rearrangement of a wafer, it becomes possible to suppress processing dispersion of the back process by dispersion in a residual membrane.

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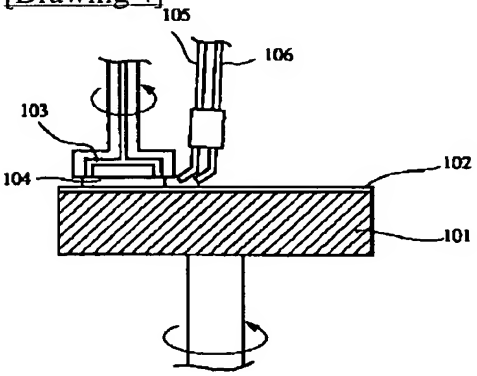
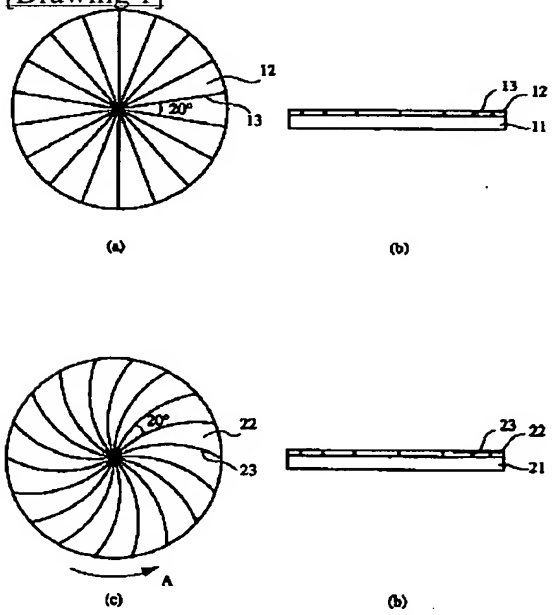
DRAWINGS

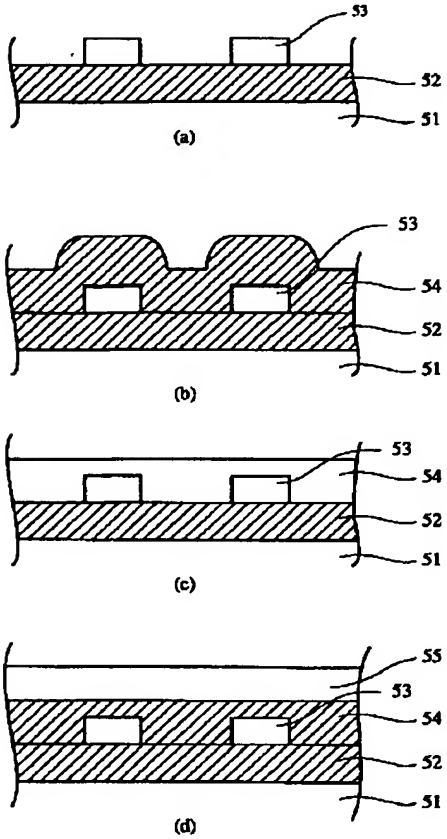
[Drawing 4]



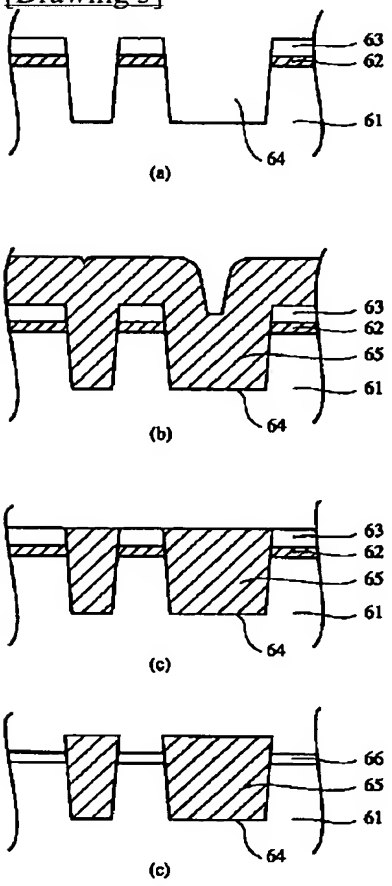
[Drawing 1]



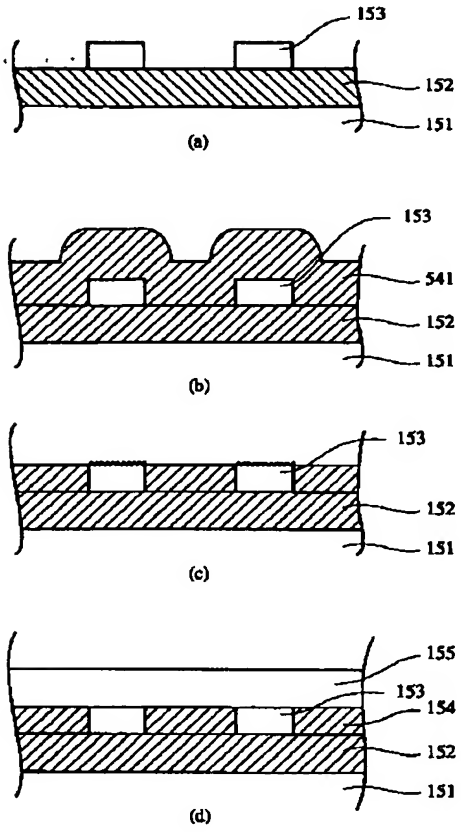
[Drawing 2]



[Drawing 3]



[Drawing 5]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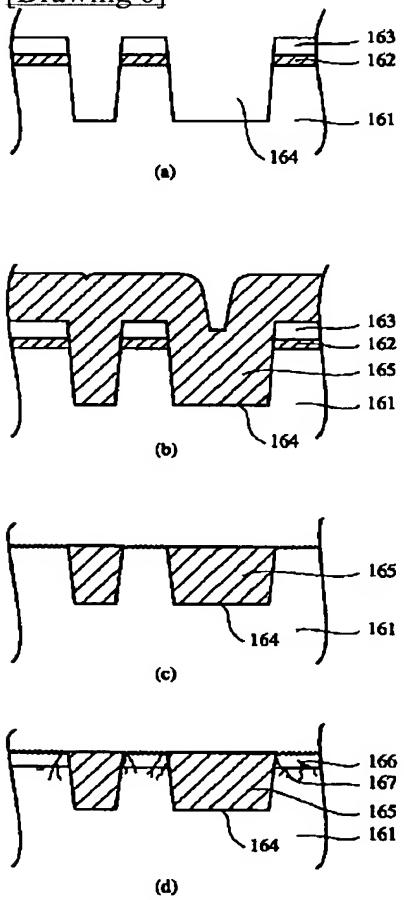
(d)

[Drawing 6]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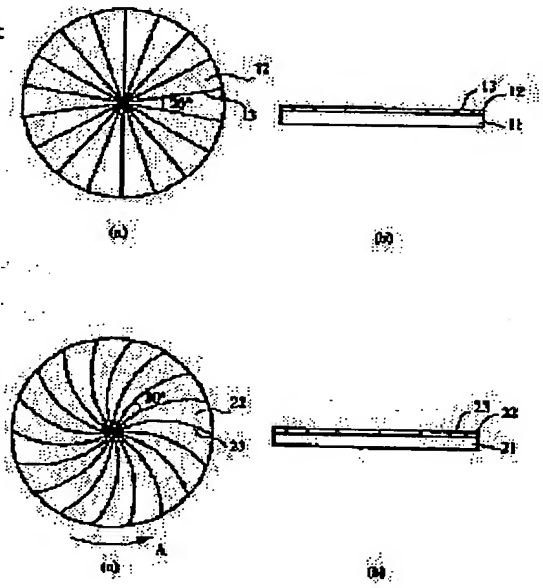
CONSTITUTION: The structure of an abrasive cloth is constituted of a several mm-thick polyurethane 11 and about 1mm-thick abrasive pads 12 adhered oh the surface of the polyurethane 11. The fan-shaped abrasive pads 12 are adhered on the surface of the polyurethane 11. Intervals of 2mm or thereabouts are respectively provided between the pads 12 so that an abrasive liquid flows well, whereby grooves 13 are provided in the abrasive cloth in a radial form from the center of the abrasive cloth. Thereby, the abrasive liquid flows from the central part of a platen to the outer periphery of the platen via the grooves provided in the abrasive cloth by a centrifugal force which is generated by the rotation of the platen.



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37/04	Ｚ			
			Ｈ０１Ｌ　21/ 88	Ｋ

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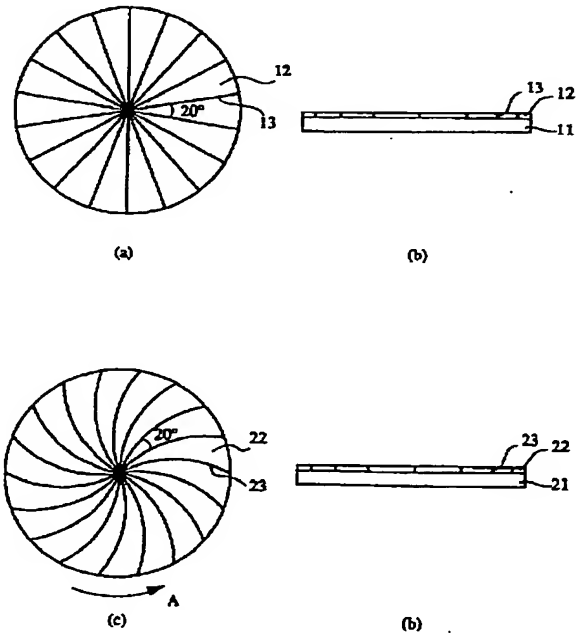
(54)【発明の名称】　半導体装置の製造方法と研磨装置

(57)【要約】

【構成】　本発明においては、研磨装置のプラテン上に貼られる研磨布に放射状の溝１３を設け、研磨液のはけを向上させ、ウエハの周辺部と中央部で研磨量の差が生じない構造とする。併せてこの研磨装置を用いて、ウエハ上の層間膜の平坦化工程や、埋め込み素子分離膜の平坦化工程を行う。

【効果】　本発明によれば研磨液のはけが向上するために、ウエハの周辺部と中央部で研磨量の差が少なく平坦化を行うことが可能となる。層間膜の平坦化工程においては、層間膜が研磨されすぎることがなく、配線間のショートを防ぐことができる。また素子分離膜の平坦化工程においては、ウエハが研磨されることがなく、ウエハの転位によるジャンクションリークの発生を防ぐことが可能となる。



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【特許請求の範囲】

【請求項１】　表面に段差を有する半導体基板を用意する工程と、
前記段差表面上に絶縁層を形成する工程と、
放射状に溝を有する研磨布により前記絶縁膜を研磨する工程とを具備することを特徴とする半導体装置の製造方法。

【請求項２】　半導体基板内の所定の導電型領域と接続された導電層を形成する工程と、
前記導電層を被覆する絶縁層を形成する工程と、
前記配線層を被覆して前記半導体基板上に絶縁層を形成する工程と、
放射状に溝を有する研磨布で前記絶縁膜を研磨する工程とを具備することを特徴とする半導体装置の製造方法。

【請求項３】　所定の導電型の半導体基板を用意する工程と、
前記半導体基板の所定の領域に溝を形成する工程と、
前記溝の内部を含む前記半導体基板表面上に絶縁膜を形成する工程と、
放射状に溝を有する研磨布で前記絶縁膜を研磨する工程とを具備することを特徴とする半導体装置の製造方法。

【請求項４】　請求項１または２または３記載の半導体装置の製造方法において、　前記研磨布の放射状の溝は、前記研磨布の回転方向に対し反対方向へ湾曲していることを特徴とする半導体装置の製造方法。

【請求項５】　請求項１または２または３記載の半導体装置の製造方法において、　前記絶縁膜を研磨する工程は、研磨液による化学的研磨と、研磨液と研磨布による機械的研磨により行われることを特徴とする半導体装置の製造方法。

【請求項６】　導電層と前記導電層を被覆する絶縁層を有する基板を支持する基板支持部と、前記基板表面を研磨する研磨布と、前記研磨布を着脱可能に固定した定盤と、前記基板と前記研磨布とを相対的に回転摺動させる回転機構とを有する研磨装置において、
前記研磨布は放射状の溝を有していることを特徴とする研磨装置。

【請求項７】　請求項６記載の研磨装置において、
前記研磨布の放射状の溝は、前記プラテンの回転方向に対し反対方向へ湾曲していることを特徴とする研磨装置。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は半導体装置の製造方法と研磨装置、特に平坦化技術を要する半導体装置の製造方法と研磨装置に関する。

【０００２】

【従来の技術】近年半導体素子の微細化や素子に形成される配線の多層化が進んでいる。よって半導体基板（以下、ウエハと称する。）表面を平坦化し、微細化や配線

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の多層化を促進するために平坦化技術の向上が要求されている。この平坦化技術の中でＣＭＰ（Chemical and Mechanical Polishing）法はその効果やコストの面で有効な技術とされている。ＣＭＰ法は、研磨液に化学的に被研磨材をエッチングする能力を持たせ研磨を行うと同時に、研磨液に含まれる粒子により機械的に被研磨材を研磨する方法である。

【０００３】続いてＣＭＰ法に用いられる研磨装置の構造について、図４を参照して説明する。研磨装置は研磨台とウエハを固定するウエハ保持部、研磨液を供給する部分を有し、研磨台はプラテン１０１（定盤）とその表面上に貼られた研磨布１０２を有している。またウエハ保持部はバキューム穴１０３よりウエハ１０４を吸引することによりウエハを固定する。研磨液を供給する部分はスラリー用ノズル１０５と純水ノズル１０６を有している。

【０００４】ウエハの平坦化工程においては、上記のウエハ保持部とプラテンがともに回転し、ウエハ保持部が下降しウエハの表面をプラテン上の研磨布に接触させ加圧することにより行われる。この工程においては、ウエハの表面状態を考慮し化学的研磨のエッチング量と、機械的研磨の加圧のバランスを最適化することが重要である。化学的研磨の研磨量は研磨液の種類、ｐＨ、組成等の条件によって決定される。また機械的研磨の研磨量は研磨液に含まれる粒子の種類や濃度、研磨布、圧力、回転速度、回転方向等の条件によって決定される。

【０００５】しかし上記の条件を制御することは容易ではなく、ウエハ間によってまたは同一のウエハ内において研磨量にばらつきが生じる。特に同一ウエハ内の研磨量のばらつきはウエハの中央部において研磨量が多くなるというものであり、この原因としては、研磨液がウエハの中央部に溜まり易く、このためウエハの中央部において研磨量が多くなるためにウエハ中央部が速く研磨されてしまうためである。これを防ぐための有効な対策が少なくその制御は困難である。よって半導体装置の製造工程においては、次に示すような問題点が生じる。

【０００６】まず第一の例として半導体装置の製造工程において、層間膜の平坦化工程においてＣＭＰ法を適用する場合について図５を参照して説明する。まず図５（ａ）に示すように、ウエハ１５１表面上に第一の層間膜１５２が成膜されており、第一の配線層１５３を形成するために、６０００オングストロームのＡｌ膜を成膜しこれをパターニングする。

【０００７】続いて図５（ｂ）に示すように、Ａｌ膜１５３表面上と露出している第一の層間膜１５２表面上に、第二の層間膜１５４として膜厚１００００オングストロームのシリコン酸化膜を成膜する。この後、ＣＭＰ法を用い第二の層間膜の平坦化を行う。

【０００８】平坦化工程が終了したウエハの中央部では、研磨液が多く溜まり研磨量が多くなるために、図５

（ｃ）に示すように、第一の配線層１５３上の第二の層間膜１５３が研磨されすぎ、第一の配線層１５３の表面がむき出しになる場合がある。

【０００９】この状態で表面に第二の配線層１５５としてＡｌ膜を成膜すると、図５（ｄ）に示すように、ウエハの中央部では第一の配線層１５３と第二の配線層１５５が接触し第一の配線層と第二の配線層がショートするという問題が生じる。

【００１０】例えウエハの中央部において第一の配線層１５３の表面がむき出しにならなくとも、ウエハの中央部と周辺部では第二の層間膜１５４の研磨量が異なり、ウエハ１５１からの層間膜１５２、１５４の膜厚に差が生じてしまう。この状態で例えばウエハ１５１とのコンタクトを形成しようとする場合、ウエハ１５１の中央部と周辺部でのＲＩＥ法によるエッチングの制御が困難であり、層間膜１５２、１５４の膜厚が厚い周辺部に合わせて、エッチングを行うと層間膜１５２、１５４の膜厚が薄い中央部では、エッチングがウエハ１５１まで達し、ウエハにダメージを与えてしまう。逆に、層間膜１５２、１５４の膜厚が薄い中央部に合わせてエッチングを行うと、層間膜1-52、１５４の膜厚が厚い周辺部では、層間膜１５２、１５４に十分な深さのコンタクトを形成する異が困難となる。

【００１１】また第二の例として半導体装置の製造工程における、埋め込み素子分離層の平坦化工程において、ＣＭＰ法を適用する場合について図６を参照して説明する。まず図６（ａ）に示すように、ウエハ１６１表面上に膜厚５００オングストロームの酸化膜１６２を介して、ストッパー膜として膜厚２０００オングストロームの多結晶シリコン膜１６３を成膜し、素子分離層の形成予定領域上の多結晶シリコン膜１６３、酸化膜１６２、ウエハ１６１をＲＩＥ（Reactive Ion Ecthing）法によりエッチングし、深さ６０００オングストローム程度のトレンチ１６４を形成する。

【００１２】続いて図６（ｂ）に示すように、埋め込み材として膜厚１００００オングストロームの酸化膜１６５を、トレンチ内及び多結晶シリコン膜１６３表面上に成膜する。この後、ＣＭＰ法を用い酸化膜１６５の平坦化を行う。

【００１３】平坦化工程が終了したウエハの周辺部では、ストッパー膜である多結晶シリコン膜１６３を残し、平坦化工程は終了されるが、ウエハの中央部においては図６（ｃ）に示すように、研磨液が多く溜まり研磨量が多くなるために、多結晶シリコン膜１６３は完全に研磨されウエハ１６１までが研磨される場合がある。

【００１４】この状態で通常と同様に半導体装置の製造を続けると、多結晶シリコン膜１６３と酸化膜１６２を剥離するために行うエッチングにおいて、ウエハの中央部ではウエハ表面が露出しているために、ウエハ１６１がエッチングされダメージを受ける。このため図６

（ｄ）に示すように、ウエハ中央部特に素子分離層との境界部のウエハにおいて、欠陥が生じ、転位１６７が生じている場合がある。不純物領域１６６を形成するためのイオン注入工程を行う場合においては、この転位１６７はジャンクションリーク電流を発生させるという問題が生じる。

【００１５】従ってウエハ１６１が研磨されすぎるのを防ぐために、ウエハの中央部と周辺部での研磨量のばらつきを考慮し、このばらつきが大きいほど多結晶シリコン膜１６３の膜厚を厚くする厚くする必要がある。

【００１６】しかしながら、ウエハ１６１の中央部と周辺部で多結晶シリコン膜１６３や酸化膜１６２の研磨量が異なっている場合、これらを除去すると埋め込み素子層として形成されている酸化膜１６５の周辺に、ウエハ１６１の中央部と周辺部で異なった高さの段差が生じる。例えば、ウエハ１６１上にＷＳｉ等の導電膜を堆積しこれをパターニングした場合は、この段差が高いウエハ１６１の周辺部では、段差の側壁に導電膜が残留することとなり、この残留した導電膜がショートする等の問題が生じる。

【００１７】上記のように従来の研磨装置を用いたＣＭＰ法による半導体装置の製造工程においては、被研磨材を研磨する研磨液がウエハの中央部に多く残留し、ウエハの周辺部と中央部で研磨量が異なる。このため、例えば層間膜の平坦化工程を行うと、ウエハ中央部において層間膜が研磨されすぎ、配線間のショートが生じたり、コンタクトを形成する場合には、十分な深さのコンタクトを形成できない場合や逆に、ウエハをエッチングしてしまう場合がある。

【００１８】また埋め込み素子分離膜の平坦化を行うと、ウエハの中央部においてウエハが研磨され、これによりウエハ内に転位が生じ、不純物領域を形成するとウエハ内の転位を原因とするジャンクションリークが発生する場合や、埋め込み素子層上に形成された導電膜をパターニングする場合は、この導電膜が残留してしまいショートが生じる場合がある。

【００１９】

【発明が解決しようとする課題】本発明は上記の問題点を鑑み、ウエハの周辺部と中央部においてその研磨量に差が生じないような研磨装置と、その研磨装置を用い配線間のショートや、転位によるジャンクションリーク電流の発生を防ぐ半導体装置の製造方法を提供することを目的とする。

【００２０】

【課題を解決するための手段】上記の目的を達成するために本発明においては、研磨液がウエハの中央部で多く溜まることを防ぐために、研磨装置のプラテン上に貼られる研磨布に放射状の溝を設け、研磨液のはけを向上させ、ウエハの周辺部と中央部で研磨量の差が生じない構造とする。併せてこの研磨装置を用いて、ウエハ上の層

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間膜の平坦化工程や、埋め込み素子分離膜の平坦化工程を行う。

【００２１】

【作用】本発明によれば、半導体装置の製造工程において、研磨装置を用いてウエハ上の層間膜の平坦化工程や、埋め込み素子分離膜の平坦化工程を行う場合に、研磨装置のプラテン上に貼られる研磨布に、研磨液のはけを向上させるために放射状の溝を設けることにより、ウエハの周辺部と中央部で研磨量の差が少なく平坦化を行うことが可能となる。よって層間膜の平坦化工程においては、層間膜が研磨されすぎることがなく、配線間のショートを防ぐことができる。また素子分離膜の平坦化工程においては、ウエハが研磨されることがなく、ウエハの転位によるジャンクションリークの発生を防ぐことが可能となる。さらに研磨後の残膜のばらつきによる後の工程で生じる加工のばらつきを抑えることが可能となる。

【００２２】

【実施例】本発明の実施例について図面を参照して説明する。まず本発明の研磨装置の第一の実施例における研磨布の上面図を図１（ａ）に、横面図を図１（ｂ）に示す。また研磨布以外の研磨装置に関しては、従来と同様であり説明図は省略する。研磨布の素材は従来と同様である。

【００２３】研磨布の構造は、厚さ数ｍｍのポリウレタン１１とその表面に張り付けられた厚さ１ｍｍ程度の研磨パッド１２から構成されており、ポリウレタン１１の表面上に、中心角２０度の１６枚の扇形の研磨パッド１２が張り付けられている。各扇形の研磨パッド１２間は研磨液のはけが良くなるように、２ｍｍ程度の間隔を有しており、よって研磨布の中心より放射状に合計１６本の溝１３を有している。　これにより研磨液はプラテンの回転によって生じる遠心力によって、プラテンの中心部より研磨布の間の溝を経由して外周へ流れるために、平坦化工程が行われているウエハの中心部に研磨液が多く溜まることがなくなり、ウエハの周辺部と中心部で研磨量の差が生じるという問題点が解決される。

【００２４】続いて本発明の第二の実施例における研磨布の上面図を図１（ｃ）に、横面図を図１（ｄ）に示す。第二の実施例は第一の実施例と同様の素材によるものであり、研磨パッドの溝の形状が異なるものである。第二の実施例におけるポリウレタン２１表面上の研磨パッド２２は、一定方向に湾曲した放射状の溝２３を有し、第一の実施例と同様に中心角２０度の１２枚の研磨パッドより構成されており、各研磨パッド間では２ｍｍ程度の間隔を有しており、よって研磨布の中心より湾曲した放射状に合計１６本の溝を有している。第一の実施例と同様の効果が得られるが、矢印Ａで示すプラテンの回転方向と反対方向へ湾曲した溝を形成することにより、さらに研磨液のはけが良くなる。

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【００２５】上記実施例においては、研磨布はポリウレタンと研磨パッドとの２層により構成されている例を示したが、研磨布を研磨パッド１層で構成しても良い。この場合厚さ１～２ｍｍ程度の研磨パッド上に深さ０．５～１ｍｍ程度の溝を形成する。また、研磨パッドにより形成する溝の本数や溝の形成間隔は、上記に示した本数や角度に限定されることはなく、プラテンやウエハ支持部の回転速度や被研磨面の状態、研磨液の種類や濃度等の違いにより種々変形して実施することが可能である。

【００２６】また第二の実施例においては、研磨パッドにより形成する溝に湾曲を持たせて形成する例を示したが、湾曲度についても、プラテンやウエハ支持部の回転速度、研磨液の種類や濃度等の違いにより種々変形して実施することが可能である。

【００２７】続いて上記に示した研磨装置を用いて、半導体装置の製造工程において平坦化工程を行う場合の実施例を図面を参照して説明する。まず製造方法の第一の実施例としては図２（ａ）に示すように、ウエハ５１表面上に第一の層間膜５２が成膜されており、第一の配線層５３を形成するために、６０００オングストロームのＡｌ膜を成膜しこれをエッチングしパターニングを行う。

【００２８】続いて図２（ｂ）に示すように、Ａｌ膜５３表面上と露出している第一の層間膜５２表面上に、第二の層間膜５４として膜厚１００００オングストロームのシリコン酸化膜を成膜する。この後、本発明による研磨装置にウエハをセットし、これを動作させＣＭＰ法による第二の層間膜の平坦化を行う。

【００２９】平坦化工程が終了したウエハの中心部と周辺部では、研磨パッドに形成されている溝の働きにより研磨液がウエハ中央部に多く溜まることがなく、基板の中央部と周辺部で研磨量の差が減少し、ウエハの中央部と周辺部で共に、図２（ｃ）に示すように第一の配線層５３表面上に第二の層間膜５４が残る構造を得ることができる。

【００３０】続いて図２（ｄ）に示すように、第二の配線層５５がＡｌ膜を成膜することにより形成される。層間膜５４は第一の配線層５３上に形成されているため、配線間の所望の耐圧は保たれる。

【００３１】次に製造方法の第二の実施例として半導体装置の製造工程における、埋め込み素子分離層の平坦化工程においてＣＭＰ法を適用する場合について図３を参照して説明する。

【００３２】まず図３（ａ）に示すように、ウエハ６１表面上に膜厚５００オングストロームの酸化膜６２を介して、ポリッシングのストッパー膜として膜厚２０００オングストロームの多結晶シリコン膜６３を成膜し、素子分離層の形成予定領域上の多結晶シリコン膜６３、酸化膜６２、ウエハ６１をエッチングし、深さ６０００オングストローム程度のトレンチ６４を形成する。

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【００３３】続いて図３（ｂ）に示すように、埋め込み材として膜厚１００００オングストロームの酸化膜６５をトレンチ内及び多結晶シリコン膜６３表面上に成膜する。この後、本発明による研磨装置にウエハ６１をセットし、これを動作させ酸化膜６５の平坦化を行う。

【００３４】平坦化工程が終了したウエハの中心部と周辺部では、研磨パッドに形成されている溝の働きにより研磨液がウエハ中央部に多く溜まることがなく、ウエハの中央部と周辺部での研磨量の差が減少し、ほぼ均一に平坦化を行うことができる。ウエハの中央部と周辺部で共に図３（ｃ）に示すように、ウエハが研磨されることがない。

【００３５】続いて図３（ｄ）に示すように、多結晶シリコン膜６３と酸化膜６２をエッチングにより除去し、ウエハ６１の所定の領域に不純物を注入し不純物領域６６を形成する。

【００３６】これら上記層間膜の平坦化工程において、本発明による研磨装置を用いることで、ウエハの周辺部と中央部で研磨量の差を減少させることができる。よって多結晶シリコン膜や酸化膜を除去するために用いられるエッチングによって、ウエハがダメージを受けることがなく、またウエハ内に転位が生じず不純物領域を形成してもジャンクションリークを生じることがなく、さらに配線層間のショートが生じない等、信頼性の高いウエハの平坦化を行うことができる。

【００３７】

【発明の効果】本発明によればプラテン上に貼られるれる研磨布に、放射状の溝を設けることにより研磨液のはけが向上する。よってウエハの周辺部と中央部で研磨量の差が少なく平坦化を行うことが可能となる。例えば層間膜の平坦化工程においては、層間膜が研磨されすぎることがなく、また素子分離膜の平坦化工程においては、半導体ウエハが研磨されることがなく、配線間のショートやウエハの転位によるジャンクションリーク電流の発＊

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＊生を防ぐことが可能となると共に、残膜のばらつきによる後工程の加工ばらつきを抑えることが可能となる。

【図面の簡単な説明】

【図１】本発明の製造装置の実施例における上面図及び断面図。

【図２】本発明の製造装置による製造方法を説明する断面図。

【図３】本発明の製造装置による製造方法を説明する断面図。

【図４】研磨装置の外観図。

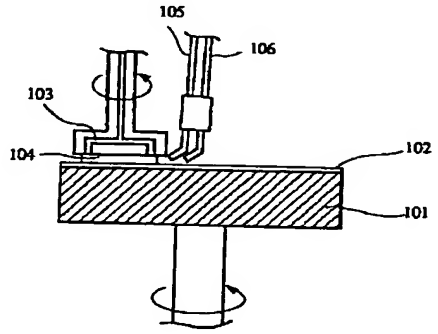
【図５】従来の製造装置による製造方法を説明する断面図。

【図６】従来の製造装置による製造方法を説明する断面図。

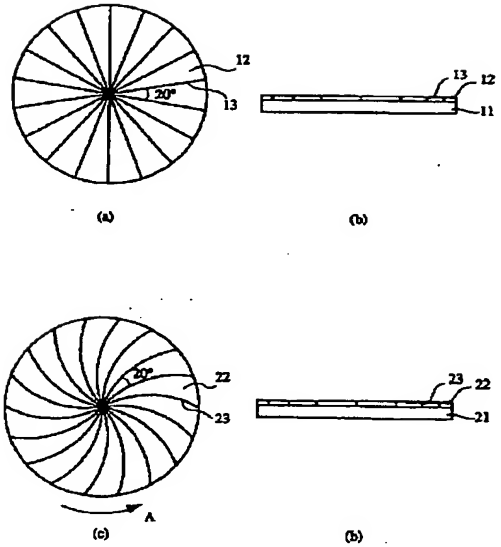
【符号の説明】

１１、２１　ポリウレタン
１２、２２　研磨パッド
１３、２３　研磨パッドの溝
５１、６１、１５１、１６１　ウエハ
５２、１５２　第一の層間膜
５３、１５３　第一の配線層
５４、１５４　第二の層間膜
５５、１５５　第二の配線層
６２、６５、１６２、１６５　酸化膜
６３、１６３　多結晶シリコン膜
６４、１６４　トレンチ
６６、１６６　不純物領域
１０１　プラテン
１０２　研磨布
１０３　バキューム穴
１０４　ウエハ
１０５　スラリー用ノズル
１０６　純水ノズル
１６７　転位

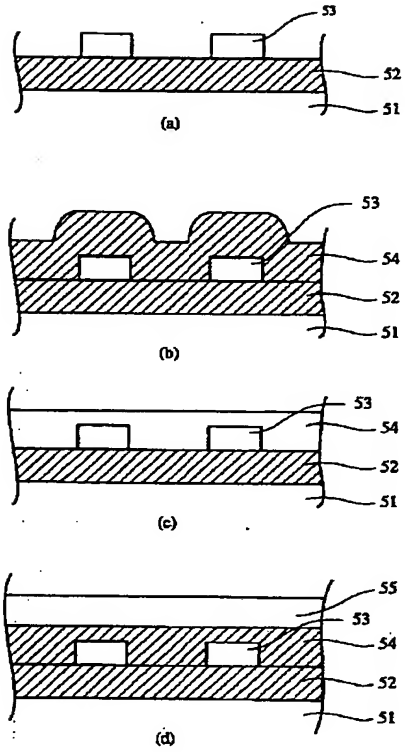
【図４】



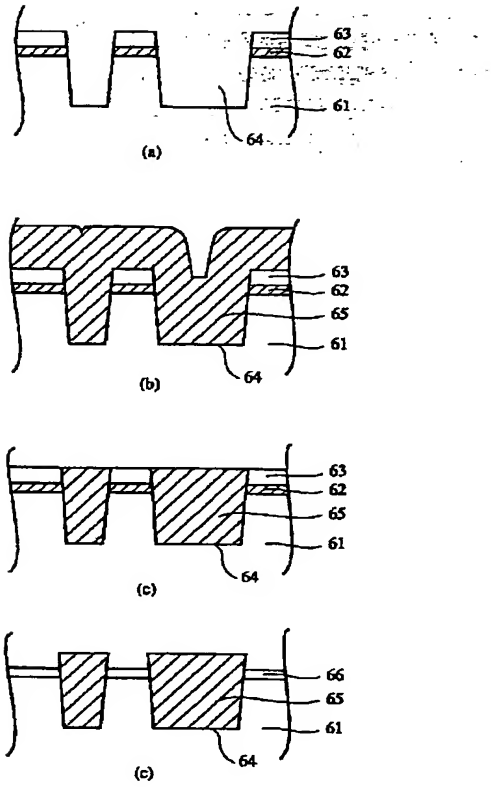
【図１】


12
20°
13
13
12
11
(a)
(b)
20°
22
23
23
22
21
A
(c)
(b)

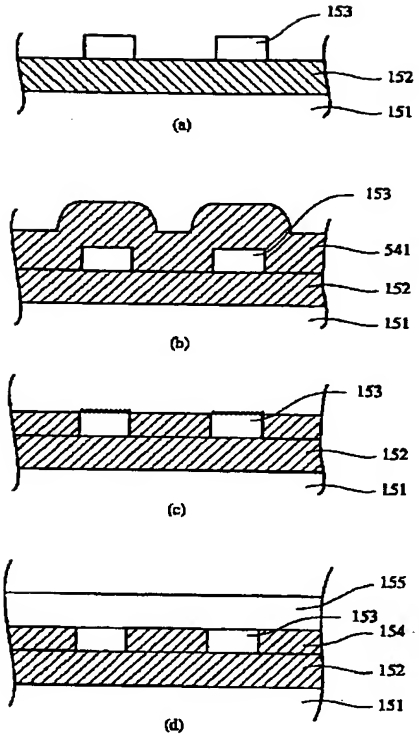
【図２】


53
52
51
(a)
53
54
52
51
(b)
53
54
52
51
(c)
55
53
54
52
51
(d)

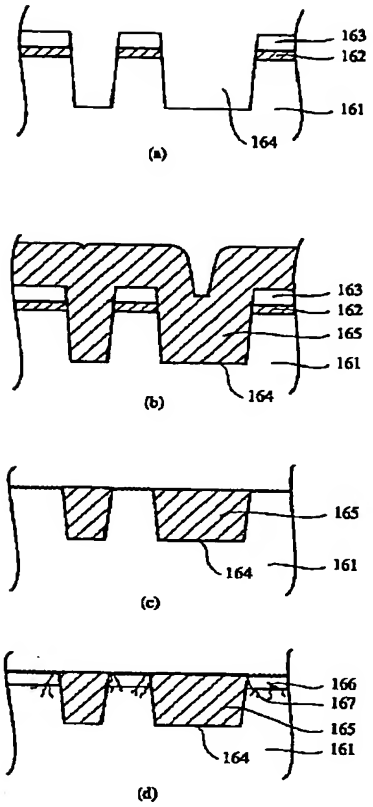
【図３】


63
62
61
64
(a)
63
62
65
61
64
(b)
63
62
65
61
64
(c)
66
65
61
64
(c)

【図５】



【図６】



フロントページの続き

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